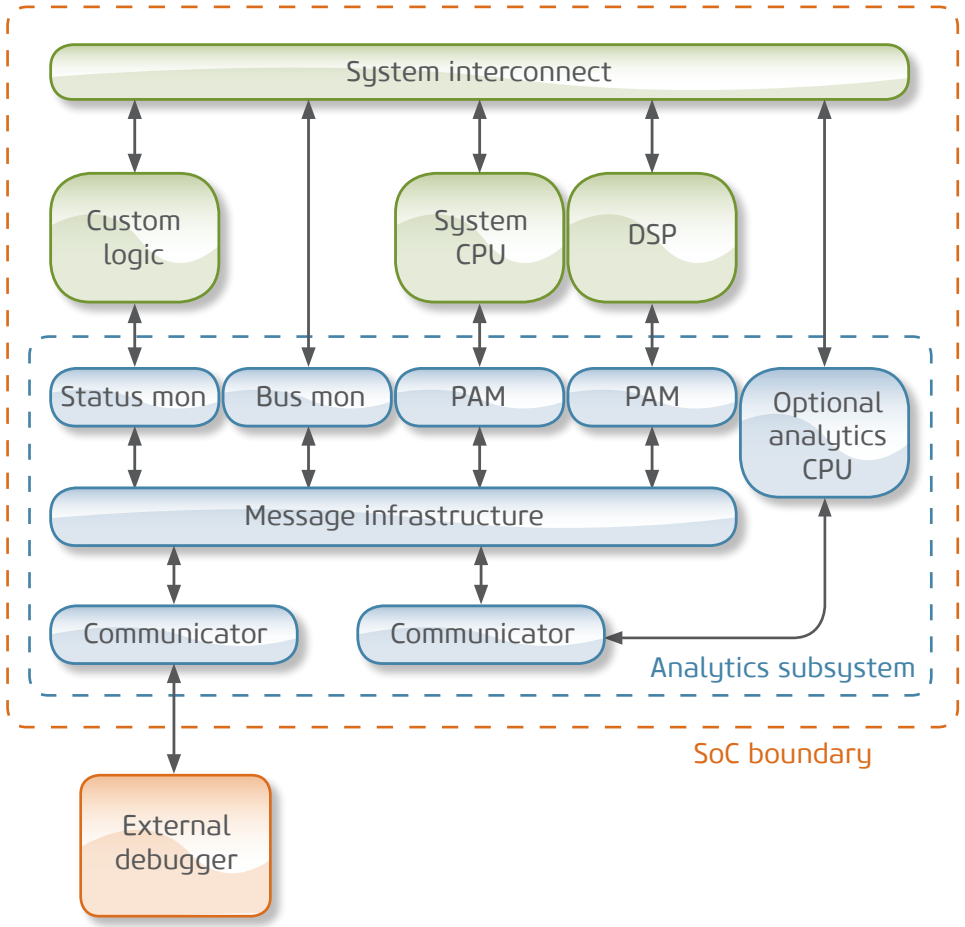
SoC debug, analytics and security

UltraSoC provides a complete suite of silicon IP and software for post-silicon debug, performance monitoring, optimization, analytics and hardware-based security. It is vendor-independent, works non-intrusively and at wire speed. The UltraSoC portfolio includes IP blocks to support all major CPUs, protocol-aware probes for common buses and interconnects and support for custom logic.



UltraSoC provides a holistic, system-level view of the complex behaviors within today's SoCs that helps engineers develop and optimize SoC hardware and software in the lab and in-field.

By incorporating UltraSoC IP into a device, designers can intelligently monitor, understand and control the activity of any on-chip structure – including custom logic, buses, and CPU cores from leading vendors such as ARM, MIPS, CEVA and Cadence/Tensilica.

UltraSoC turns on-chip data into actionable information, accelerating SoC time-to-revenue; revealing hard-to-find bugs; increasing quality; de-risking development and reducing potential liability costs. It fits gracefully into any SoC development flow and is fully compatible with tools such as Eclipse, GDB, Lauterbach and Teledyne Lecroy.

With low overhead of silicon area and power, the UltraSoC architecture scales from low-cost embedded chips to the largest SoC project, easing the development of heterogeneous multicore designs with hundreds of hardware blocks and substantial amounts of software.

At-a-glance

- **Scalable SoC monitoring / analytics**
- **Silicon IP + software tools**
- **CPU vendor independent**
- **Non-intrusive, wire speed**
- **Reduces post-silicon debug burden**
- **Reveals hard-to-find bugs, deadlocks**
- **Enables system optimization**
  - Power
  - CPU resource
- **In-field applications**
  - Hardware-based security
  - Performance monitoring
  - SLA enforcement

Functional overview

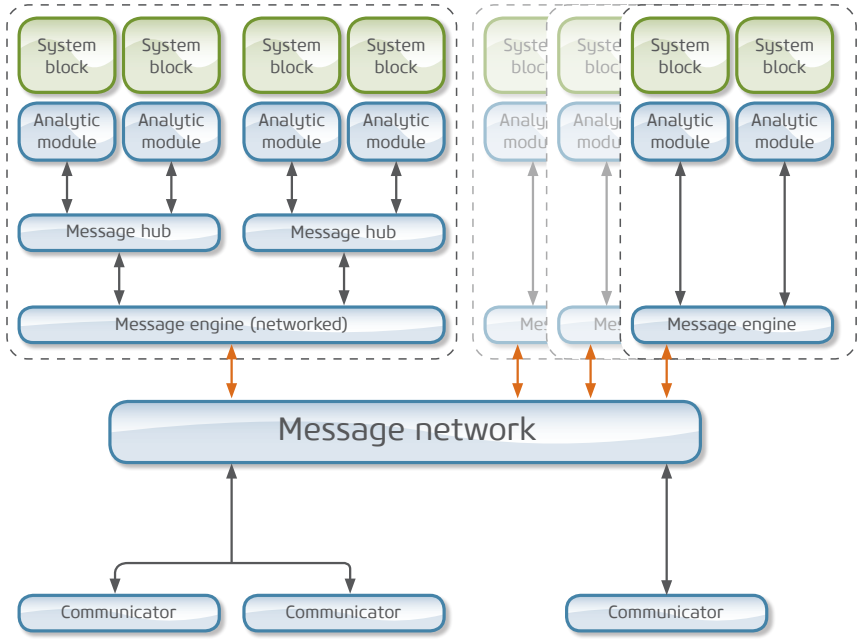
The modular, hierarchical UltraSoC architecture consists of three classes of IP block:

- Analytic modules: enable monitoring and control of system components
- Message infrastructure: dedicated fabric to connect UltraSoC components
- Communicators: interface the UltraSoC system to on-chip or external systems

Analytic modules can probe system hardware or software. Some non-intrusively monitor system buses (both master and slave); others offer a memory-mapped peripheral device API for access by software; others are optimized to interface with CPUs; and some are "embedded logic analyzers" for monitoring custom logic. All are parameterized at design time and configurable at run time through the message infrastructure.

The message infrastructure is a dedicated, scalable message-based interconnect fabric that is easy to route while enabling low-latency signaling and cross-triggering – without interfering with the system buses or interconnect.

Communicator modules connect the UltraSoC environment to external systems either on- or off-chip. They include lightweight peripheral interfaces; high-performance trace interconnects; versatile blocks such as the Universal Streaming Communicator; and industry-standard interfaces such as JTAG and USB.



Product Features

- **On-chip monitoring and analytics IP**
  - Delivered as parameterized soft cores
- **Matching, filtering, sequencing, trace and event generation**
- **Monitor master or slave interface on a bus, point-to-point fabric or on-chip network**
- **CPU run control**
  - Breakpoints, performance monitoring, trace, cross triggering, etc
  - Optimized support for ARM, Cadence/Tensilica, Synopsys/ARC, MIPS, CEVA and other CPUs
- **Rich message-based infrastructure**
  - Support for power domains and clock domains
  - Optimizations for timing closure
- **On- and off-chip interfaces**
  - Vendors' debug systems (CoreSight, PDTrace)
  - DMA controller
  - Bus slave interface with on-chip software
  - Universal Streaming Communicator: IEEE1149, SWD-style, Aurora, SerDes
  - USB: non-intrusively via system USB port
  - Generic: Parallel; JTAG; Virtual console/UART