

Maithil Pachchigar

Applications Engineer
Analog Devices, Inc.

Richard Liggiero

Chief Engineer,
LTX-Credence

GET ADC DATA BEYOND THE DATA SHEET

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Abstract

When selecting a high resolution ADC for a design, you often need to know about characteristics that may not be traditionally published in the data sheet. Take, for example, converter's noise performance over all codes. You may not find this specification in a data sheet. Fortunately, we designers now have a tool that can analyze ADCs for this and other parameters and evaluate the true performance of the converter from a system level perspective.

ATE system manufacturer LTX-Credence (LTXC) has developed the Signature Analysis toolset that can analyze converter products such as the AD7960 class, designed for high end instrumentation and ATE. The toolset is designed for systems that require careful analysis of the transfer function or direct measurements of the output based on performance over all codes rather than the typical shorted inputs or at several other distinct converter levels.

When selecting an ADC, you may have to consider overall ADC efficiency, power, size, and price. In addition, pay close attention to the static and dynamic performance over the Nyquist bandwidth. This article introduces a toolset to help see outside the data sheet, which will help lead to a decision to select a precision ADC for that new system design to be rolled out. We will now demonstrate the performance of the Analog Devices AD7960, an 18-bit PulSAR® ADC, using the Signature Analysis toolset.

AD7960

The AD7960, an 18-bit, 5 MSPS differential ADC, shown in Figure 1, uses CAPDAC (capacitive digital-to-analog converter) technology to reduce noise and improve linearity without adding latency or pipeline delay. The AD7960 returns to the acquisition mode about 100 ns after the start of conversion and its acquisition time is approximately 50% of the total cycle time. So it has nearly the same acquisition time despite being twice as fast as the next fastest 18-bit SAR ADC. This makes the AD7960 easy to drive and relaxes the burden on the ADC driver's settling time requirement. It offers the wide bandwidth, high accuracy (INL: ±0.8 LSB, SNR: 99 dB, and THD: -117 dB typical), and fast sampling (200 ns) required for high end data acquisition systems while reducing power dissipation and cost in multichannel applications.

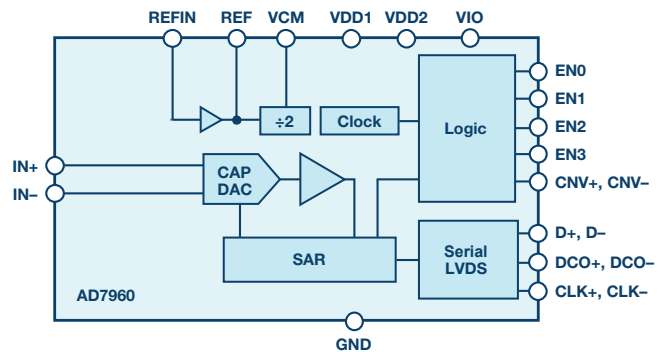


Figure 1. AD7960 functional block diagram shows the CAPDAC as part of the SAR (successive approximation register) loop.

The AD7960 series digital interface uses LVDS (low voltage differential signaling), offering self clocked and echoed clock modes that provide high speed data transfer up to 300 MHz (CLK± and D±) between the ADC and the digital host. The LVDS interface reduces the number of digital signals and eases signal routing because several devices can share a common clock. This also reduces power dissipation, which is especially useful in multiplexed applications.

The self clocked mode simplifies the interface with the host processor, allowing complex timing with a header that synchronizes the data from each conversion. This mode is especially beneficial when using many ADCs per system and where board space, power dissipation, and layout routing constraints are present. A header is required to allow the digital host to acquire the data output because there is no clock output synchronous to the data. The echoed clock mode is useful when using a few ADCs per system without any board space or power consumption constraints. This mode offers robust timing at the expense of an extra differential pair (DCO±).

The AD7960 operates from 1.8 V and 5 V power supplies, dissipating only 39 mW at 5 MSPS when converting in self clocked mode and 46.5 mW at 5 MSPS when converting in echoed clock mode. Its power dissipation scales linearly with sample rate, as shown in Figure 2, making it a good fit for low power applications. The power dissipation at very slow sample rates is dominated by the LVDS static power.

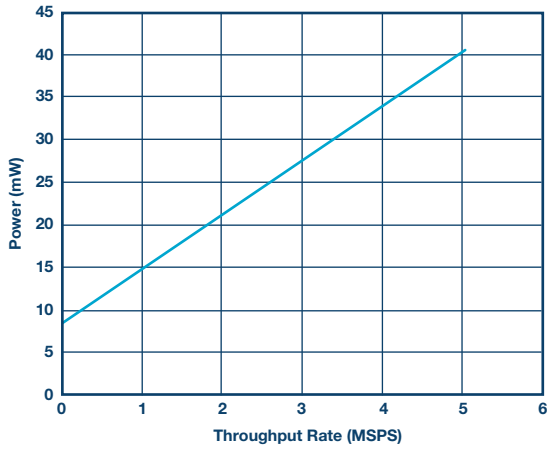


Figure 2. The AD7960's power consumption vs. throughput rate is linear.

The AD7960 series lets you use any of three external reference options: 2.048 V, 4.096 V, and 5 V. An on-chip buffer doubles the 2.048 V reference voltage, so the conversions are referred to 4.096 V or 5 V.

Signature Analysis Toolset

With the idea of getting to the data outside the traditional data sheet, we present a simplified view of the Signature Analysis toolset interacting with an ADC. Today's data sheets are quite similar in performance and structure because the converter market has reached a point where performance often gets traded off for price and power. But at what expense are those trade-offs? Here we focus on identifying a converter's true performance.

The Signature Analysis toolset has algorithms that push the data analysis to where we can evaluate the true performance of the converter beyond what's traditionally published in data sheets. The toolset was initially developed as an evaluation vehicle to specify next-generation components for LTXC's data converter test module (DCTM). As a direct result of the success of the DCTM, the toolset provides a method to verify, specify, and characterize converters over all codes. The DCTM and data processing algorithms, specifically developed for converter testing, lets IC manufacturers add value to their products. As the best-in-class mixed-signal channel card, the DCTM surpasses familiar standard bench instrumentation when evaluating a converter's performance and the trade-offs in performance, power, and price.

The Signature Analysis toolset provides valuable insight into an ADC's transfer function (as shown in Figure 3), which can help end users select a particular converter. This insight also offers the product development team precise feedback on the deviations of the converter's transfer function from those of an ideal converter. Identifying perturbations in the transfer function is a familiar concept. However, the ability to isolate where they occur has proven to be invaluable to the system development process.

AD7960 Evaluation

Presented here is the kind of information learned about the converter using the LTX-Credence Signature Analysis toolset.

Linearity and dynamic performance are two important test requirements for high resolution precision converters. These tests are analyzed and displayed for the AD7960 using the toolset and plotted in Figure 4. These parameters are also found in the AD7960 data sheet.

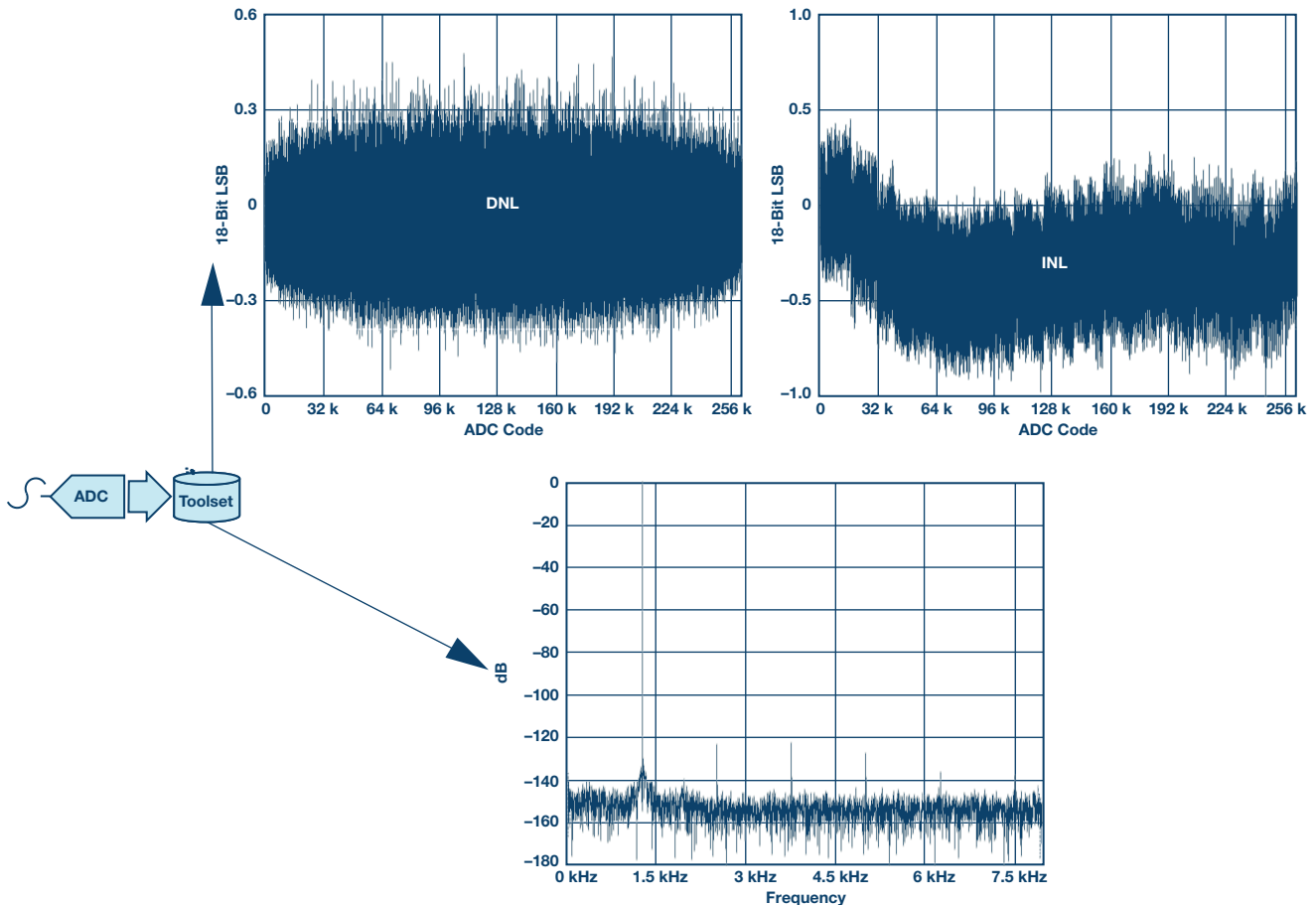


Figure 3. Data flow using the Signature Analysis toolset produces several plots.

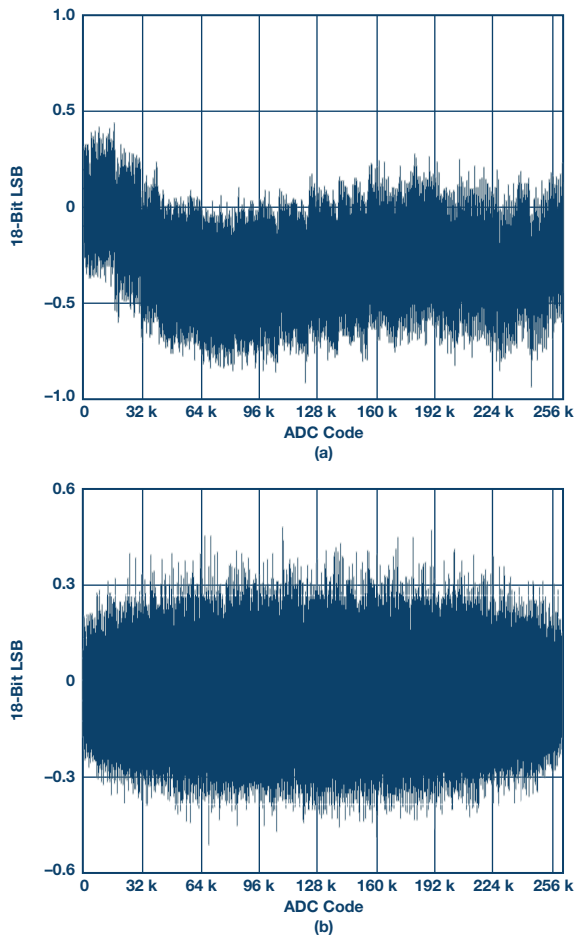


Figure 4. AD7960 static performance for linearity plots of (a) INL and (b) DNL.

The signal integrity and performance of the test equipment’s analog instrumentation is critical in determining the quality of the AD7960, as well as the entire data acquisition system. This fact about signal integrity is sometimes lost in translation when viewing the converter’s end results. The tester’s signal conditioning network, reference design, and power supply do contribute to the overall measured performance in Figure 5.

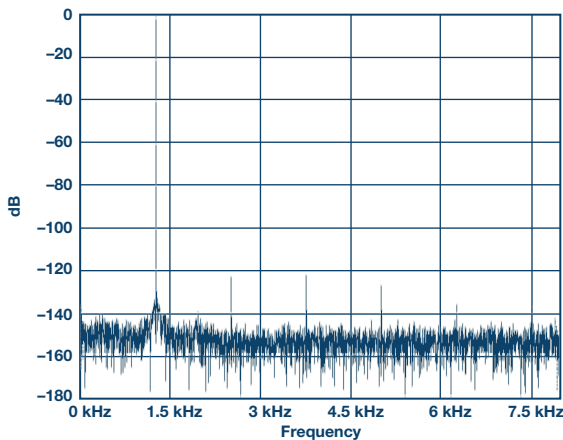


Figure 5. The AD7960 dynamic performance, measured using the Signature Analysis toolset, shows THD = 119.8 dB, SNR = 99.2 dBFS, and ENOB of 16.2 bits.

Postprocessing the AD7960’s data set with the Signature Analysis toolset lets you find the converter’s noise performance over its full-scale range. LTCX has developed a method to reconstruct the high resolution converter noise over all codes, as shown in Figure 6.

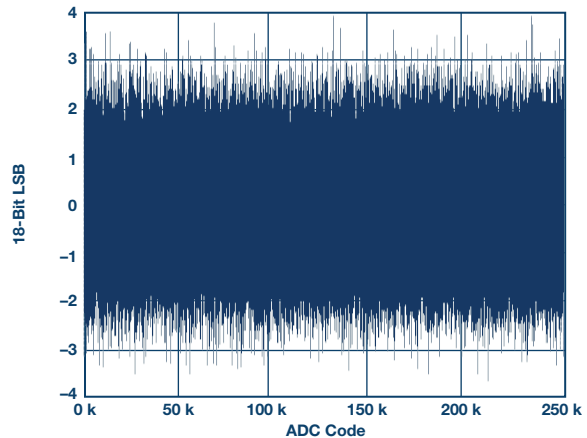


Figure 6. This plot of AD7960 noise response includes data at all ADC codes.

In terms of enhancing product appeal through the published data sheet, we can characterize the converter’s noise performance over all ADC codes rather than the typical shorted inputs or at several other distinct converter levels. This method provides a more inclusive view of the converter, as well as of the acquisition system.

From this information set gathered with the toolset, you can ascertain stability, predict SNR, its repeatability and reproducibility, and potential noise issues as a function of code. This extended data is missing from today’s data sheets, which could aid designers in selecting a converter that is used extensively across all codes. In addition to using the toolset as a feedback mechanism to help differentiate future system level designs, it is also used as a demonstration tool to show the converter’s signal integrity.

To summarize the point, Figure 6 shows the AD7960 derived noise over all codes (262, 144, 218). This type of noise response is something that single code histograms are unable to reveal. This is important in practical usage from a system level perspective. For example, ATE manufacturers use the converter over its entire transfer function rather than a single code method, thereby enhancing the converter’s appeal to system level designers.

As is the case with the AD7960, Figure 6 shows no apparent shift in the transfer function or any specific discontinuity, thus demonstrating system capability. Digging deeper from the noise plot in Figure 6, the SNR can be derived using the following equation:

$$SNR = 20 \times \log_{10} \left\{ \frac{2^{ADC_Res}}{2\sqrt{2} \cdot ADC_Noise} \right\} = 20 \times \log_{10} \left\{ \frac{2^{18}}{2\sqrt{2} \cdot 0.86 \text{ LSB rms}} \right\} = 100.7 \text{ dBFS}$$

The measured SNR is 99.2 dBFS, as shown in Figure 5. This offers a correlation level of all codes noise tested to within 1.5 dB of the calculated 100.7 dB noise level to the equation. Also, built into the toolset is the capability to postprocess the information for a finer view of the real performance of the AD7960.

Conclusion

System level designers evaluating high end converters will find these types of results invaluable in their converter selection process as they navigate trade-offs among key metrics of performance, power, and price. Using the Signature Analysis toolset, you can intuitively look at the specifications beyond of the traditional data sheet and identify key parametric performance metrics to feedback, improve, and validate next-generation instrumentation design.

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About The Author

Maithil Pachchigar is an applications engineer within the precision converters business unit at Analog Devices. He joined ADI in 2010 and supports the precision ADC product portfolio and customers in the industrial, instrumentation, medical, and energy segments. Having worked in the semiconductor industry since 2005, Maithil has published several technical articles. He received an M.S.E.E. degree from San Jose State University in 2006 and an M.B.A. from Silicon Valley University in 2010. He can be reached at maithil.pachchigar@analog.com.

Richard Liggiero is a chief engineer at LTX-Credence. Joining LTX-Credence in June of 2006, he has led the mixed-signal test applications team in developing next-generation test methods and test techniques. He is a participating member of the IEEE TC-10 standards committee for ADC/DAC specification, Tau Beta Pi, and Eta Kappa Nu. He has a master's degree from Northeastern University and holds two patents. He also has over 20 years of experience in the semiconductor industry, as he continues to focus LTX-Credence innovative technology in ultraprecision analog measurement and signaling technology to new markets. He can be reached at richard_liggiero@ltxc.com.

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Analog Devices, Inc. Worldwide Headquarters

Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643, U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc. Europe Headquarters

Analog Devices, Inc.
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc. Japan Headquarters

Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc. Asia Pacific Headquarters

Analog Devices
5F, Sandhill Plaza
2290 Zuchongzhi Road
Zhangjiang Hi-Tech Park
Pudong New District
Shanghai, China 201203
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

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