TECHNOLOGY WHITE PAPER

Backplane Ethernet: Enabling High-Performance Embedded Systems

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Introduction

Ethernet has grown to become a universal networking technology, evolving to provide ever faster links over a wide range of media. To meet the need for higher performance, many embedded systems now use "backplane Ethernet" to communicate between cards in modular systems. This paper provides an overview of the benefits of backplane Ethernet and highlights the key concerns for VPX system designers.

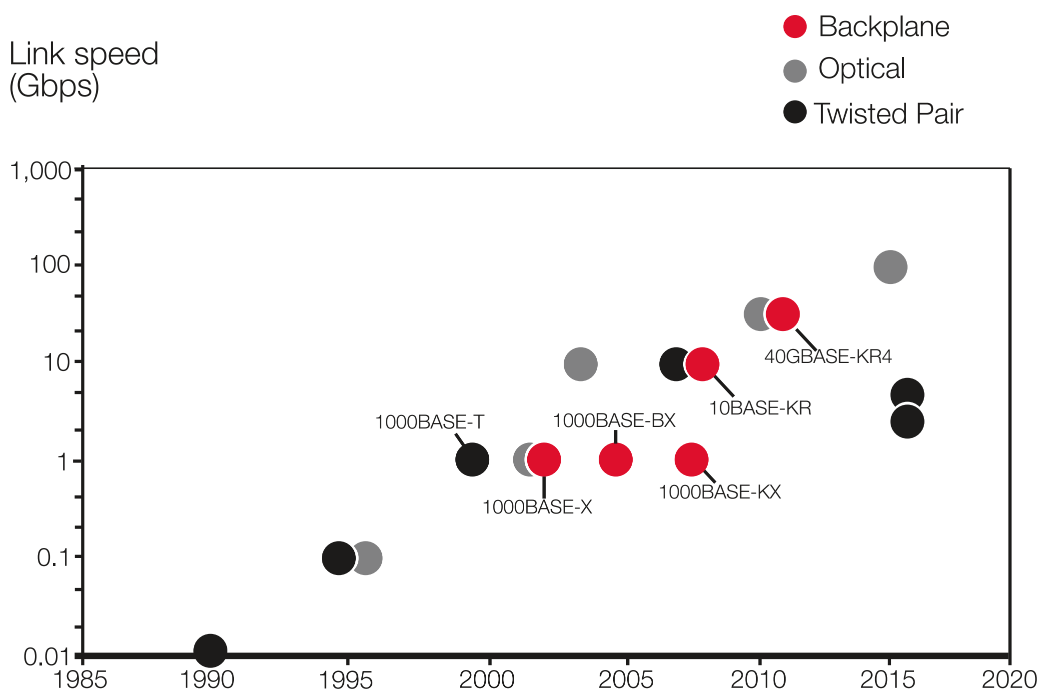

Figure 1: Selected Ethernet standards

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Background

Ethernet has long been used to provide connectivity within embedded systems. In many cases the Ethernet interface on embedded products is based on the same standard commonly deployed on personal computers and other commercial devices: 1000BASE-T "Gigabit Ethernet". However a variety of other Ethernet standards provide numerous alternatives suitable for different applications. These other standards vary in performance (with speeds ranging from 10 Mbps to 100 Gbps), and the media they use (such as twisted pair cabling, or fiber optics). Relatively new "backplane" Ethernet standards enable high-speed links over PCBs, through connectors and backplanes. These link standards provide a number of advantages for modular embedded systems that connect together multiple processor cards, in particular modern high-performance embedded computing (HPEC) systems based on the VPX standard.

Before Backplane Ethernet

Widely deployed in a variety of commercial applications, 1000BASE-T provides Gigabit Ethernet over up to 100 meters of unshielded twisted pair cable. It owes its popularity to its combination of robustness, performance, and broad interoperability – thanks to careful design and years of "plugfests", connecting a device to an RJ-45 port usually "just works". Numerous features under the hood contribute to this robustness including adaptive equalization, PAM-5 signaling, and auto-MDIX to automatically fix crossover mismatches.

Because of this versatility and popularity, BASE-T has long been implemented in embedded applications to connect between modules, and to external devices. Although it is designed for use over twisted pair cabling, it works well over backplanes and through the connectors typically found in VME and VPX systems. However BASE-T Ethernet does have some drawbacks. It requires bulky transformers to provide magnetic coupling. It can require a discrete PHY or controller device, and it uses four differential pairs – two send, two receive. These drawbacks can be a concern in embedded applications where size, weight and power (SWaP) are critical.

An alternative to BASE-T is so-called "SerDes" Ethernet, which requires only two signal pairs (one send and one receive). Originally used for chip-to-chip communications on boards, several related standards have been defined. For embedded systems, all offer the same benefits relative to BASE-T – fewer parts and pins are needed to provide Gigabit Ethernet. On 3U VPX cards where board space and backplane differential pairs are scarce, switching from BASE-T to SerDes can double the number of ports available on a switch module.

Standard	Data Rate	Symbol Rate	Line Coding	Standardized
1000BASE-X	1 Gbps	1.25 Gbaud	8B/10B	IEEE 802.3z
1000BASE-BX	1 Gbps	1.25 Gbaud	8B/10B	PICMG ATCA 3.1
1000BASE-KX	1 Gbps	1.25 Gbaud	8B/10B	IEEE 802.3ap
SGMII	1 Gbps	625 MHz DDR	8B/10B	-
10GBASE-KR	10 Gbps	10.3125 GHz	64B/66B	IEEE 802.3ap

Table 1 - Selected SerDes Ethernet Standards

SGMII, 1000BASE-X and 1000BASE-BX

SerDes Gigabit Ethernet encompasses a number of related but subtly different standards. Early specifications for Gigabit Ethernet defined several flavors of optical Ethernet such as 1000BASE-LX and 1000BASE-SX. These optical links share a signaling and encoding layer commonly referred to as "BASE-X". For this reason many devices designed to connect to optical transceivers offer a "BASE-X" mode. Similarly, devices intended to connect to an optical or BASE-T PHY device may offer an SGMII option. SGMII is a specification for connections between separate MAC and PHY devices that also leverages a single SerDes pair at Gigabit rates with BASE-X encoding.

Since they share the same encoding, devices based on these related BASE-X SerDes technologies can often be connected and made to work together. However since the specifications differ - notably in how they detect and negotiate link parameters - interoperability is not guaranteed. To address this interoperability gap, a SerDes Ethernet standard was defined by the PICMG industry group: 1000BASE-BX. This was subsequently adopted by VITA as the standard for SerDes Gigabit Ethernet over backplanes in the OpenVPX standard.

Backplane Ethernet

1000BASE-T and many other Ethernet PHY types are defined by the IEEE 802.3 standard. This document has expanded over the years to enable Ethernet on a wide range of media, at ever-faster data rates, with a growing list of features. One of the key philosophies of the standard is interoperability – Ethernet devices should work together whenever possible. To enable this vision, many PHY specifications require auto-negotiation, link training and other techniques to ensure that compatible devices will link up, even if they have different capabilities and underlying technology.

With the ratification of 802.3ap in 2007, 802.3 Ethernet gained a formal PHY standard for electrical backplanes. For Gigabit Ethernet, 1000BASE-KX provides all the benefits of earlier SerDes Ethernet technology – including Gigabit performance over two differential pairs across electrical backplanes. However 1000BASE-KX also includes the capability advertisement and auto-negotiation features common to other 802.3 standards, greatly simplifying interoperability.

Newer additions to the 802.3 standard have added backplane Ethernet PHY standards for 10G, 40G and 100G data rates over one to four SerDes lanes (Table 2). In systems with high-performance modules and backplanes, 10 Gbps SerDes technology enables 10 Gigabit Ethernet over a single lane, or 40 Gigabit Ethernet over four lanes. In smaller form factors such as 3U VPX where fewer pins are available, these link types are key to enabling high-performance Ethernet switch fabrics and HPEC clusters.

IEEE 802.3 PHY type	Signaling and Speed	OpenVPX Mapping
1000BASE-KX	SerDes 1.25 Gbaud	UTP – 5.1.2
10GBASE-KR	SerDes 10.3 Gbaud	UTP – 5.1.7
10GBASE-KX4	SerDes 4x 3.125 Gbaud	FP – 5.1.5
40GBASE-KR4	SerDes 4x 10.3 Gbaud	FP – 5.1.8

Table 2 - IEEE 802.3 Backplane Ethernet PHY Standards

Since all of the 802.3 backplane Ethernet PHY standards include auto-negotiation, it is possible to connect two devices that have different native PHY types. Based on their capabilities, the two will negotiate to use the best connection supported by both. The scheme for advertising capabilities and deciding the greatest common type is defined in 802.3 clause 73 (Table 3).

Priority	Technology	Capability
1	100GBASE-CR10	100 Gbps 10 lane, highest priority
2	40GBASE-CR4	40 Gbps 4 lane
3	40GBASE-KR4	40 Gbps 4 lane
4	10GBASE-KR	10 Gbps 1 lane
5	10GBASE-KX4	10 Gbps 4 lane
6	1000BASE-KX	1 Gbps 1 lane, lowest priority

Table 3 - 802.3 Cl. 73 Priority

Other benefits of the IEEE 802.3 backplane Ethernet standards include well-defined signal integrity requirements and forward error correction for high speed links. These channel parameters have been adapted for VPX as part of the VITA 68 specification.

Ethernet and OpenVPX

Profiles have been defined in VITA65 (OpenVPX) that map backplane Ethernet to standard module profiles. Many current profiles map 1000BASE-BX SerDes to two-pair Ultra-Thin Pipes (UTP) to provide “control plane” Gigabit Ethernet. 1000BASE-KX may also be used provided that auto-negotiation is disabled to enable compatibility with 1000BASE-BX.

Future editions of the standard are expected to include control plane and data plane based on 10GBASE-KR and 40GBASE-KR4 Ethernet.

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Curtiss-Wright Defense Solutions Ethernet Switching Products for Embedded Systems

Curtiss-Wright has a wide range of Ethernet switching and routing modules for the rugged embedded market. Many of these modules provide backplane Ethernet interfaces at 1, 10 and 40 Gbps (Table 4).

Product	Form Factor	Description	SerDes & Backplane Ethernet Support
VPX3-652	VPX 3U	Low-power managed Gigabit Ethernet switch	8x 1000BASE-KX SerDes(optional)
VPX3-683	VPX 3U	Managed multi-layer Gigabit Ethernet switch	24x 1000BASE-X SerDes
VPX3-685	VPX 3U	Secure router/switch with firewall and VPN services	8x 1000BASE-X SerDes (optional)
VPX3-687	VPX 3U	High density 10 Gbps backplane Ethernet switch	2x 40GBASE-KR4 24x 10GBASE-KR
VPX6-6902	VPX 6U	SRIO fabric and Gigabit Ethernet switch	20x 1000BASE-X SerDes
VPX6-6802	VPX 6U	Fabric40 Ethernet and InfiniBand switch	16x 40GBASE-KR4 20x 1000BASE-X SerDes
PMC-651 XMC-651	PMC XMC	Gigabit Ethernet switch mezzanine	4x 1000BASE-X SerDes (optional)

Table 4 - Curtiss-Wright Ethernet Switching & Routing Modules

Learn More

White Paper: Embedded Ethernet Physical Layer Standards (2016)

Product Guide: Switching and Routing Product Guide

Products: Networking Cards

References

1. IEEE 802.3-2012 Standard, https://standards.ieee.org/about/get/802/802.3.html

2. VITA 65 https://www.curtisswrightds.com/technologies/open-architecture/openvpx-architecture.html

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